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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/217,213	12/21/1998	MARK I. GARDNER	5500-05001	8618

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/217,213	GARDNER ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-27 and 30-32* is/are rejected.

7)☒ Claim(s) *28 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. The Amendment filed December 21, 2004 has been entered. Claims 18, 19, 22, 24 and 26 have been amended. Claims 27-32 have been added. Thus, Claims 18-32 are pending.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 18-21, 27 and 30 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 21 of U.S. Patent No. **6,599,810**. Although the conflicting claims are not identical, they are not patentably distinct from each other because the product produced by the method of claim 20 of patent '810 includes all limitations of the conflicted claims.

4. Claims 22-26, 27, 31 and 32 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 5, 6 and 8 of U.S. Patent No. **6,433,400**. Although the conflicting claims are not identical, they are not patentably distinct

from each other because the barrier atoms of patent '400 also incorporated at the portions of the substrate adjacent to the trench under a layer.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 18-21, 27 and 30 are rejected under 35 U.S.C. 102(a) as being anticipated by Son et al. (U.S. Patent No. 5,904,538).

Son teaches an isolation structure laterally disposed between a first active region and a second active region of a semiconductor substrate as claimed including:

a trench (26) formed within semiconductor substrate (21);

a thermally grown oxide layer (27) having a first portion disposed across a bottom of trench (26) and second and third portions (sidewalls) disposed within trench (26) laterally adjacent to the first and second active regions;

a deposited oxide (28) disposed within trench (26) above the first portion and between the second and third portions (sidewalls), the deposited oxide (28) having an upper surface which is approximately coplanar with the upper surface of semiconductor substrate (21); and

implanted silicon atoms (25a) arranged within regions of the first and second active regions proximate the upper surface of the substrate (21) and laterally adjacent to the second and third portions of the thermally grown oxide (27), wherein the implanted silicon atoms fill vacancies and interstitial sites within the semiconductor substrate (21) resulting from formation of trench (26). (See Fig. 2G).

Product by process limitation:

The expression "implanted" as recited in claims 18, and 27, is/are taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a

"product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Note that Applicant has burden of proof in such cases as the above case law makes clear.

The silicon atoms (25a) of Son are implanted thus, should inherently fill the vacancies and interstitial sites.

With respect to claim 19, the silicon atoms of Son are arranged within the first and second active regions directly beneath a spacer or layer (22).

Note that the term "spacer" is broadly directed to a "layer" of material. As a device, the silicon atoms are inserted into the substrate adjacent to the trench and under a layer, thus, the limitation of the claim is met.

With respect to claim 20, the spacer or layer (22) of Son extends from a sidewall of the trench (26) and residing over the semiconductor substrate (21).

With respect to claim 21, since the spacer or layer (22) of Son is formed on the active region, extending from the opening, thus, the limitation is met.

With respect to claim 27, Son teaches an integrated circuit as claimed including:

a semiconductor substrate (21) having a trench isolation structure (26) formed therein;

active regions (either side of trench 26) within the semiconductor substrate (21) extending to opposing edges of the trench isolation structure (26); and

implanted silicon (25a) or barrier atoms arranged within the semiconductor substrate at each of the opposing edges of the trench isolation structure (26), wherein the implanted silicon or barrier atoms fill vacancies and interstitial sites within the semiconductor substrate resulting from formation of the trench isolation structure (26). (See Fig. 2G).

The silicon atoms (25a) of Son are implanted thus, should inherently fill the vacancies and interstitial sites.

With respect to claim 30, only implanted silicon atoms (25a) of Son are arranged within the semiconductor substrate at each of the opposing edges of the trench isolation structure to fill vacancies and interstitial sites within the semiconductor substrate resulting from formation of the trench isolation structure.

6. Claims 22-27, 31 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Gardner et al. (U.S. Patent No. 5,811,347).

With respect to claim 22, Gardner teaches a semiconductor topography as claimed including:

a dielectric filled trench (112) arranged within a semiconductor substrate (102); and

barrier atoms (nitrogen) arranged within the semiconductor substrate (102) beneath a layer (104) that extends above a portion of the semiconductor substrate (102), wherein the barrier atoms (nitrogen) fill vacancies and interstitial sites within the semiconductor substrate resulting from formation of the trench (112). (See Fig. 8).

Regarding the spacer, a similar reasoning as that of claim 19 also applies.

Regarding the term "fill vacancies and interstitial sites", since the barrier atoms (nitrogen) of Gardner are implanted thus, should inherently fill the vacancies and interstitial sites.

With respect to claim 23, the spacer or layer (104) of Gardner is configured laterally between a peripheral of the trench (112) and continuously covering the active regions.

With respect to claim 24, the spacer or layer (104) of Gardner is made of a different material (104) than the dielectric (126) of the dielectric filled trench (112).

With respect to claim 25, the barrier atoms of Gardner are selected from the group consisting of nitrogen.

With respect to claim 26, the barrier atoms of Gardner are arranged within an active region of the semiconductor substrate (102) adjacent to the trench (112) thus, within 0.1 micron.

With respect to claim 27, Gardner teaches an integrated circuit as claimed including:

a semiconductor substrate (102) having a trench isolation structure (112) formed therein;

active regions (either side of trench 112) within the semiconductor substrate (102) extending to opposing edges of the trench isolation structure (112); and

implanted barrier atoms (nitrogen) arranged within the semiconductor substrate at each of the opposing edges of the trench isolation structure (112), wherein the implanted barrier atoms fill vacancies and interstitial sites within the semiconductor substrate resulting from formation of the trench isolation structure (26). (See Fig. 8).

The barrier atoms of Gardner are implanted thus, should inherently fill the vacancies and interstitial sites.

With respect to claim 31, only barrier atoms (atoms) of Gardner are arranged within the semiconductor substrate (102) at each of the opposing edges (128) of the trench isolation structure (112) to fill vacancies and interstitial sites within the semiconductor substrate (102) resulting from formation of the trench isolation structure.

With respect to claim 32, the barrier atoms of Gardner are nitrogen.

Allowable Subject Matter

7. Claims 28 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: prior art of record fails to teaches an integrated circuit in the combination of the limitations as claimed including both silicon and barrier atoms are incorporated into the edges of the trench.

Response to Arguments

9. Applicant's arguments with respect to claims 18-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

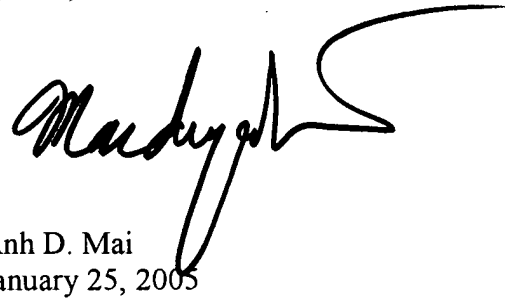
10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Anh D. Mai
January 25, 2005